



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/837,995

04/19/2001

Shubhendu S. Mukherjee

1662-36900 JMH
(P00-3156)

8856

23505

7590

02/27/2004

CONLEY ROSE, P.C.

P. O. BOX 3267

HOUSTON, TX 77253-3267

EXAMINER

DAMIANO, ANNE L

ART UNIT

PAPER NUMBER

2114

DATE MAILED: 02/27/2004

5

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/837,995

Applicant(s)

MUKHERJEE ET AL.

Examiner

Anne L Damiano

Art Unit

2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 April 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13 is/are allowed.
- 6) ☒ Claim(s) 1,4,5,8-12 and 14-18 is/are rejected.
- 7) ☒ Claim(s) 2,3,6 and 7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 July 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 and 3. 6) ☐ Other: _____

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jonathan M. Harris (Req. No. 44,144) on February 18th, 2004.

The application has been amended as follows:

Page 1, paragraph 3, insert --09/839,626-- after "Serial No."

Page 1, paragraph 3, delete "(Attorney Docket No. 1662-37400)" before "filed concurrently herewith."

Page 1, paragraph 4, insert --09/839,459-- after "Serial No."

Page 1, paragraph 4, delete "(Attorney Docket No. 1662-37000)" before "filed concurrently herewith."

Page 1, paragraph 5, insert --09/836,621-- after "Serial No."

Page 1, paragraph 5, delete "(Attorney Docket No. 1662-37100)" before "filed concurrently herewith."

Page 2, paragraph 6, insert --09/838,078-- after "Serial No."

Page 2, paragraph 6, delete "(Attorney Docket No. 1662-37200)" before "filed concurrently herewith."

Art Unit: 2114

Page 2, paragraph 7, insert --09/838,069-- after "Serial No."

Page 2, paragraph 7, delete "(Attorney Docket No. 1662-37300)" before "filed concurrently herewith."

Page 2, paragraph 8, insert --09/839,624-- after "Serial No."

Page 2, paragraph 8, delete "(Attorney Docket No. 1662-37500)" before "filed concurrently herewith."

Page 9, paragraph 29, line 4, replace "102" with --104-- after "Fetch unit."

Page 9, paragraph 29, line 5, replace "102" with --104-- after "fetch unit."

Page 9, paragraph 29, line 8, replace "102" with --104-- after "thread by the fetch unit."

Page 10, paragraph 30, line 1, replace "102" with --104-- after "Fetch unit."

Page 10, paragraph 30, line 1, replace "102" with --104-- after "permits the fetch unit."

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

It does not identify the city and either state or foreign country of residence of each inventor. The residence information may be provided on either on an application data sheet or supplemental oath or declaration.

Drawings

3. Figure 2 is objected to because INT UNIT lacks a component number, 142. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Allowable Subject Matter

4. Claim 13 is allowed.

The following is an examiner's statement of reasons for allowance:

The primary reason for allowance of claim 13 is the inclusion of a processor detects transient faults by verifying as between the leading and trailing threads only the committed stores and uncached memory read requests, in a pipelined, simultaneous and redundantly threaded processor, comprising: a fetch unit that fetches instructions from a plurality of threads of instructions; an instruction cache coupled to said fetch unit and storing instructions to be decoded and executed; and decode logic coupled to said instruction cache to decode the type of instructions stored in said instruction cache; wherein the processor processes a set of instructions in a leading thread and also in a trailing thread, and wherein the instructions in the trailing thread are substantially identical to the instructions in the leading thread, the instructions in the trailing thread beginning processing through the processor after the corresponding instructions in the leading thread begin processing through the processor; as recited in the claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Claims 2, 3, 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1 and 4 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 5, respectively, of copending Application No. 09/839,626. Although the conflicting claims are not identical, they are not patentably distinct from each other because both claims essentially read word for word excluding one comparable word.

These are provisional obviousness-type double patenting rejections because the conflicting claims have not in fact been patented

Regarding instant claim 1, both claims claim: A computer system, comprising: a pipelined, simultaneous and redundantly threaded ("SRT") processor having at least two threads; an input/output ("I/O") controller coupled to said processor; an I/O device coupled to said I/O controller; and a system memory coupled to said processor; wherein said SRT processor comprises: a load/store execution unit having a queue adapted to store a memory request submitted the at least two threads, wherein the memory requests directly or indirectly change values in the system memory; a compare logic coupled to said load/store execution unit that scans the contents of said read queue for corresponding memory requests generated by the at least two threads, and verifies that each corresponding memory request matches; and wherein said compare logic, based on whether the corresponding memory requests match, performs one of 1) allowing the memory request to execute, and 2) initiating fault recovery.

However, the instant application claims the queue being a store queue and 09/839,626 claims a read queue. Both store memory requests submitted by the threads and both are scanned by the compare logic for corresponding memory requests. A person skilled in that art would understand that since both queues serve the same purpose of storing memory requests, both the store and read queue are essentially the same. Therefore instant claim 1 is an obvious variation of 09/839,626 claim1.

Regarding instant claim 4 and 09/839,626 claim 5, both claim computer systems as defined in respective claim 1's further comprising each of said threads of said processor performing speculative branch execution independently from the other.

Art Unit: 2114

8. Claim 5 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 7 of copending Application No. 09/839,626. Although the conflicting claims are not identical, they are not patentably distinct from each other because instant claim 5 has a one to one correspondence in wording to claim 7 of 09/839,626 besides an obvious language variation and because it is well settled that the omission of an element and its function is an obvious expedient of the remaining elements perform the same functions as before. In re Karlson, 136 USPQ 184 (CCPA 1963).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Both current claim 5 and 09/839,626 claim 7, claim a method of checking for transient faults in a pipelined, simultaneous and redundantly threaded processor having at least two threads, the method comprising verifying, as between the at least two threads, requests.

Current claim 5 claims verifying only committed store requests and data load requests from sources that are not cached, while 09/839,626 claims verifying at least data load requests from sources that are not cached. A person skilled in the art would understand that verifying only memory requests that affect the system memory includes store requests as well data load requests.

09/839,626 claim 7 also claims duplicating return data of said data load request for use by each thread. Instant claim 5 has clearly removed this function of duplicating returned data of said data load request for use by each thread as an obvious expedient.

9. Claims 8 and 9-11 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 11 and 14-16, respectively of copending Application No. 09/839626. Although the conflicting claims are not identical, they are not patentably distinct from each other because except both claims essentially read word-for-word excluding an obvious variation.

These are provisional obviousness-type double patenting rejections because the conflicting claims have not in fact been patented.

Regarding instant claim 8, it claims: a method of detecting transient faults in a simultaneously and redundantly threaded microprocessor having at least two threads, the method comprising: executing a program as a first thread; generating a first committed store request from said first thread; storing said first committed store request in a storage queue; executing the program as a second thread; generating a second committed store request from said second thread; storing said second committed store in said storage queue; checking an address and data associated with said first committed store request against an address and data associated with said second committed store request in a compare logic; and allowing one of said first and second committed store requests to execute if the checking step shows those committed store requests are exactly the same.

09/839,626 claim 11 claims the same method, however, rather than the threads generating committed store requests the threads generate input/output commands. Committed store requests are an obvious variation of input/output commands. A person skilled in the art would understand that program threads generate store requests that must be committed to the memory. A person

Art Unit: 2114

skilled in the art would have also understood that a common input/output command includes such a command as a committed store request.

Regarding instant claim 9 and 09/839,626 claim 14, both claim the methods as defined in respective claims 8 and 11 wherein executing the first and second threads further comprises executing the first thread a plurality of program steps ahead of the second thread.

Regarding instant claim 10 and 09/839,626 claim 15, both claim the methods as defined in respective claims 8 and 11 further comprising allowing each of the first and second threads to make speculative branch execution independent of the other.

Regarding instant claim 11 and 09/839,626 claim 16, both claim the methods as defined in respective claims 8 and 11 further comprising: allowing the first thread to execute program steps out of an order of the program; allowing the second thread to execute program steps out of the order of the program; and allowing each of the first and second threads to execute the program in a different order from each other.

10. Claim 12 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 17 of copending Application No. 09/839,626. Although the conflicting claims are not identical, they are not patentably distinct from each other because except both claims essentially read word for word excluding one comparable word and an obvious variation.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Regarding claim 12, both instant claim 12 and 09/839,626 claim 17, claim: a simultaneous and redundantly threaded microprocessor comprising: a first pipeline executing a first program thread; a second pipeline executing a second program thread; a queue coupled to each of said first and second pipelines; a compare circuit coupled to said queue; wherein each of said first and second program threads independently generate corresponding requests, and each thread places those requests in the queue; and wherein said compare circuit detects transient faults in operation of said first and second pipeline by comparing the requests.

However, instant claim 12 also claims comparing at least the committed store requests from each thread while 09/839,626 claim 17 claims comparing only the requests from each thread that affect data in memory outside the microprocessor. A person skilled in the art would understand that comparing only the request from each thread that affect data in memory outside the microprocessor encompasses comparing committed store requests from each thread since committed store requests affect data in the memory outside the microprocessor.

However, the instant claim 12 claims the queue being a store queue and 09/839,626 claims a read queue. Both store memory requests submitted by the threads and both are scanned by the compare logic for corresponding memory requests. A person skilled in that art would understand that since both queues serve the same purpose of storing memory requests, both the store and read queue are essentially the same.

Instant application also claims the requests are being committed store requests, while 09/839,626 claims input/output requests. Committed store requests are an obvious variation of

input/output commands. A person skilled in the art would understand that program threads generate store requests that must be committed to the memory. A person skilled in the art would have also understood that a common input/output command includes such a command as a committed store request.

11. Claims 14 and 15-17 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 19 and 22-24, respectively of copending Application No. 09/839,626. Although the conflicting claims are not identical, they are not patentably distinct from each other because except both claims essentially read word-for-word excluding an obvious language variation.

These are provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Regarding instant claim 14, it claims, A method of detecting transient faults in a simultaneous and redundantly threaded microprocessor having at least two threads, the method comprising: executing a program as a first thread; generating a first committed store request from said first thread; storing said first committed store request in a storage queue; executing the program as a second thread; generating a second committed store request from said second thread; checking an address and data associated with said first committed store request against an address and data associated with said second committed store request; and allowing one of said first and second committed store requests to execute if the checking step shows those committed store requests are exactly the same.

09/839,626 claim 19, claims the same method, however, rather than the threads generating committed store requests the threads generate input/output commands. Committed store requests are an obvious variation of input/output commands. A person skilled in the art would understand that program threads generate store requests that must be committed to the memory. A person skilled in the art would have also understood that a common input/output command includes such a command as a committed store request.

Regarding instant claim 15 and 09/839,626 claim 22, both claim method as defined in respective claims 14 and 19 wherein executing the first and second threads further comprises executing the first thread a plurality of program steps ahead of the second thread.

Regarding instant claim, 16 and 09/839,626 claim 23, both claim the methods as defined in respective claims 15 and 22 further comprising allowing each of the first and second threads to make speculative branch execution independent of the other.

Regarding instant claim 17 and 09/839,626 claim 24, both claim the method as defined in respective claim 15 and 22, further comprising: allowing the first thread to execute program steps out of an order of the program; allowing the second thread to execute program steps out of the order of the program; and allowing each of the first and second threads to execute the program in a different order from each other.

12. Claim 18 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 17 of copending Application No. 09/839,626. Although the conflicting claims are not identical, they are not patentably distinct from each other because except both claims essentially read word for word excluding one comparable word and an obvious variation.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Regarding claim 18, both instant claim 18 and 09/839,626 claim 17, claim: A simultaneous and redundantly threaded microprocessor comprising: a first pipeline executing a first program thread; a second pipeline executing a second program thread; a queue coupled to each of said first and second pipelines; a compare circuit coupled to said queue; wherein each of said first and second program threads independently generate corresponding requests, and at least the first thread places the requests in the queue; and wherein said compare circuit detects transient faults in operation of said first and second pipeline by comparing the requests.

However, instant claim 18 also claims comparing at least the committed store requests from each thread while 09/839,626 claim 17 claims comparing only the requests from each thread that affect data in memory outside the microprocessor. A person skilled in the art would understand comparing only the request from each thread that affect data in memory outside the microprocessor encompasses comparing committed store requests from each thread since committed store requests affect data in the memory outside the microprocessor.

Instant claim 18 claims the queue being a store queue and 09/839,626 claims a read queue. Both store memory requests submitted by the threads and both are scanned by the

Art Unit: 2114

compare logic for corresponding memory requests. A person skilled in that art would understand that since both queues serve the same purpose of storing memory requests, both the store and read queue are essentially the same.

Instant claim 18 also claims the requests being committed store requests, while 09/839,626 claims input/output requests. Committed store requests are an obvious variation of input/output commands. A person skilled in the art would understand that program threads generate store requests that must be committed to the memory. A person skilled in the art would have also understood that input/output commands includes such commands as committed store requests.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (703) 305-8010. The examiner can normally be reached on M-F 9-6:30 first Fridays off.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Application/Control Number: 09/837,995
Art Unit: 2114

Page 15

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ALD



SCOTT BADERMAN
PRIMARY EXAMINER